[**Programmable Communication Group**](https://sites.google.com/a/temple.edu/programmable-communication-group/)

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| Date | Friday, September 20, 2013 | | |
| Advisor | Dr. Silage | | |
| Members | Cedric Destin | Brandon Keith | Brian Thibodeau |

Headline: Make sure to scope full extent of simulation (not partial) so we don’t overlook changes to data over time.

Topics to discuss (with Silage)

* What exactly is expected from Dr. Silage for WebEx design review video? Are we uploading .wrf file or other popular file format? Who should be able to see this review video?
* What is a tolerable bit error rate for this design? (major system requirement)
* Discuss why AFC control (initiated from carrier extraction PLL filter) isn’t necessary.
* Implementing variable bit-rate random binary generator for variable frequency audio BPSK (this tests accurate filter bandwidth performance in modem simulations).

Topics to discuss (among SD team and Silage, if necessary)

* To what extent should AGC be implemented inside of the FPGA? Can it be completely implemented within the digital domain?
* Accurate bandwidth for band-pass filters and loop filters (PLL) within the Simulink models of KD2BD modem.
* Transitioning to sample-based Simulink model (crucial for when noise is introduced).
* Implementing sample-based exclusive OR.
* We might have to increase sampling frequency to something greater than 1/(1200\*64).

Dr. Silage feedback

Topics to discuss in next SD meeting

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| **Engineer** | **Status** |
| Brian Thibodeau |  |
| Cedric Destin | * Looking at the digital filters poles and difference equation   + Test the filters using AWGN * Calculate the BER |
| Brandon Keith |  |