**[Programmable Communication Group](https://sites.google.com/a/temple.edu/programmable-communication-group/)**

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| Date | Friday, September 27, 2013 | | |
| Advisor | Dr. Silage | | |
| Members | Cedric Destin | Brandon Keith | Brian Thibodeau |

Headline: Make sure to scope full extent of simulation (not partial) so we don’t overlook changes to data over time.

Topics to discuss (with Silage)

* What exactly is expected from Dr. Silage for WebEx design review video? Are we uploading .wrf file or other popular file format? Who should be able to see this review video?
* What is a tolerable bit error rate for this design? (major system requirement)
* Discuss why AFC control (initiated from carrier extraction PLL filter) isn’t necessary.
* Implementing variable bit-rate random binary generator for variable frequency audio BPSK (this tests accurate filter bandwidth performance in modem simulations).
* Third-order Costas loop used for Doppler shift correction.

Topics to discuss (among SD team and Silage, if necessary)

* To what extent should AGC be implemented inside of the FPGA? Can it be completely implemented within the digital domain?
* Accurate bandwidth for band-pass filters and loop filters (PLL) within the Simulink models of KD2BD modem.
* Transitioning to sample-based Simulink model (crucial for when noise is introduced).
* Implementing sample-based exclusive OR.
* We might have to increase sampling frequency to something greater than 1/(1200\*64).

Dr. Silage feedback

* WebEx video on 10/04/13 should be condensed version of SD meeting today w/ project background. Upload video in any file format.
* A hard value for the bit error rate was not established.
* Found document “FPGA-BASED DIGITAL PHASE-LOCKED LOOP ANALYSIS AND

IMPLEMENTATION”

* Entertain the idea of forward error correction in modem design

Topics to discuss in next SD meeting

* Implementing PLL in FPGA (besides from Costas loop).

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| **Engineer** | **Status** |
| Brian Thibodeau | * Preliminary 2nd Order Costas Loop simulation complete.   + This loop can successfully TRACK and LOCK onto a frequency range of +/- 100 Hz from carrier frequency (i.e. 1100-1300). * NOTE: because this is only 2nd order, it only tracks a CONSTANT frequency in the range of 1100-1200Hz, NOT a changing frequency. * Next steps:   + Tune phase detector (PD) and VCO gains to increase frequency range.   + Add AWGN and evaluate BER performance.   + Investigate and research 3rd order model for Doppler Shift tracking * Lastly, posted under, mainline\simulation\simulink\KB2BD\demodulator, you will find two Simulink models:   + *Costas\_loop*   + *Ideal\_BPSK\_Modulator* |
| Cedric Destin | * Looking at the digital filters poles and difference equation   + Test the filters using AWGN * Calculate the BER |
| Brandon Keith | * Variable frequency BPSK audio generator * Verifying correct bandwidth for filter and loop filter in timing recovery circuit * Converting simulation to sample-based where necessary |